



(11) **EP 0 905 838 A1**

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
31.03.1999 Bulletin 1999/13

(51) Int. Cl.⁶: **H01S 3/25, H01L 33/00,
G09G 3/14**

(21) Application number: **98117860.1**

(22) Date of filing: **21.09.1998**

(84) Designated Contracting States:
**AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE**
Designated Extension States:
AL LT LV MK RO SI

(72) Inventors:
• **Ouchi, Toshihiko**
Ohta-ku, Tokyo (JP)
• **Furukawa, Yukio**
Ohta-ku, Tokyo (JP)

(30) Priority: **30.09.1997 JP 282548/97**
07.09.1998 JP 268950/98

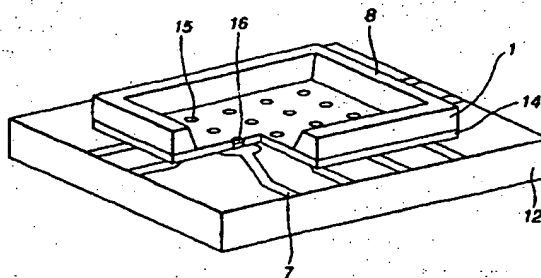
(74) Representative:
Tiedtke, Harro, Dipl.-Ing. et al
Patentanwaltbüro
Tiedtke-Bühling-Kinne & Partner
Bavariaring 4
80336 München (DE)

(71) Applicant:
CANON KABUSHIKI KAISHA
Tokyo (JP)

(54) **Surface-type optical device, fabrication method therefor and display device**

(57) A surface-type optical device, such as a surface emitting laser device, includes a first substrate, a plurality of active regions formed and disposed on the first substrate, and a control unit for injecting a current into or applying an inverse voltage to each active region. A portion of the first substrate is removed over an area including at least two active regions. The active region is constructed such that light is output from or input into each active region perpendicularly to the first substrate. A second substrate may be bonded to a side of the epitaxially-grown layers of the first substrate.

FIG.3A



BEST AVAILABLE COPY

0 905 838 A1

Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a surface-type optical device, such as a vertical cavity surface emitting laser (VCSEL), whose fabrication is easy, whose yield can be increased and which is suitable for use in a two-dimensional array structure, to its fabrication method and to a display device using the surface-type optical device.

Related Background Art

[0002] Recently, development of a solid-state light emission device of a two-dimensional array type has been desired for the purpose of its applications to large-capacity parallel optical information processing, high-speed optical connection and panel-type display apparatus. Low cost, low consumption of electric power, high productivity, and high reliability are required to achieve those applications. Various materials for such a surface emitting solid-state device have been studied and developed. It has been found that single-crystalline semiconductors are notably suitable for reliability. Especially, development of a surface emitting device using compound semiconductor has been energetically advanced. With this compound semiconductor, light emission is possible over a wide range from ultraviolet to infrared by changing materials of its substrate and layer structure. Hence, that material is prospectively seen as a display device.

[0003] Among light emission devices, a laser diode (LD) including reflection mirrors at its opposite ends is most excellent in light emitting efficiency, compared to devices using spontaneous emission. Therefore, electric power consumption can be greatly lowered when those LDs are arranged in a two-dimensional manner. With this point in view, development of the VCSEL has been actively advanced in recent years.

[0004] With the VCSEL, devices have also been developed over a range from a blue color at a wavelength of about 400 nm to a communication wavelength band of 1.55 μm . Studies have been made in material series, such as the AlGaIn/InGaIn series on a sapphire substrate, the InGaAlP/InAlP and InGaAs/AlGaAs series on a GaAs substrate, and the InGaAs/InGaAsP series on an InP substrate.

[0005] The fundamental structure of two-dimensional arrayed VCSELs is illustrated in Fig. 1. Laser light is emitted perpendicularly to a substrate 1101. Each device is provided with high-reflective coatings 1109 and 1110 of over 99% reflectivity at opposite end faces of epitaxially-grown layers with a thickness of about several microns. Reference numeral 1114 designates epitaxial layers, reference numeral 1115 designates a light

emitting region, and reference numeral 1116 designates an active layer or a light emitting portion.

[0006] A multiplicity of alternately-layered layers with different refractive indices and a common $\lambda/4$ thickness are used as the reflective mirror. The materials are generally dielectric (in the case of Fig. 1), or epitaxially-grown semiconductors. Examples of the epitaxially-grown mirror are as follows: a multi-layer mirror of alternately-formed AlAs and GaAs layers (an AlAs/GaAs mirror), an active layer and other layers are deposited on a GaAs substrate during a single growth process, as disclosed in ELECTRONICS LETTERS, 31, p. 560 (1995); and a GaAs/AlAs mirror formed on a GaAs substrate is directly or without any adhesive bonded to a laser structure of an InGaAsP/InP series grown on an InP substrate, as disclosed in APPLIED PHYSICS LETTERS, 66, p. 1030 (1995).

[0007] Further, Japanese Patent Laid-Open No. 9-223848 (1997) discloses a VCSEL with epitaxial semiconductor mirrors, in which after a structure of its epitaxial layers including an active layer grown on a semiconductor substrate is bonded to another semiconductor substrate with an integrated circuit by using polyimide adhesive or the like, its laser substrate is all removed and devices are thus separated from each other, as illustrated in Fig. 2. In such a manner, a semiconductor device with integrated VCSELs and other electric devices is fabricated. In Fig. 2, reference numeral 4100 designates a light input and output substrate, reference numeral 4100A designates a light receiving device, reference numeral 4100B designates a VCSEL, reference numerals 4100C and 4100D designate electric wires of the devices 4100A and 4100B, respectively, reference numeral 2000 designates an integrated-circuit substrate, reference numeral 2000A designates a metal wire of the integrated-circuit substrate 2000, reference numeral 3000 designates an insulating layer, and reference numeral 4000 designates an electric wire. With this construction, a high-density array is possible.

[0008] However, where a set of the epitaxial semiconductor layers is used as multi-layer mirror, the difference in refractive indices between the different semiconductor layers cannot be large in the case of InGaAsP/InP, for example. Therefore, the number of the epitaxial layers increases, and its growth time and its thickness are also increased. Thus, its productivity is lowered, and processing of the device and flattening of the surface are difficult to perform.

[0009] Further, practical materials for use as the semiconductor mirror are presently GaAs/AlAs, and when their lattice constants are considered, the choice of usable materials of the active layer is limited and its oscillation wavelength band is hence restricted. Where the GaAs/AlAs mirror is directly bonded, the size of the semiconductor substrate is limited although another wavelength band is available due to an expanded range of usable materials for the active layer. This method is

thus effective in the case of a small area only.

[0010] On the other hand, the dielectric multi-layer mirror cannot be directly laid down on the substrate, although its fabrication is easy. Therefore, the layering needs to be performed after the bottom face of the substrate 1101 is etched to open a window 1101a, as illustrated in Fig. 1. Accordingly, the window 1101a must be precisely formed, and windows 1101a cannot be formed so close to each other. As a result, its yield and uniformity are low or bad, and devices cannot be formed with high density, leading to unsuitability of the devices for a two-dimensional arrayal.

[0011] Further, also in the case of the epitaxially-grown mirror, the substrate comes to be an absorptive material depending on the oscillation wavelength band, and thus a hole must be etched in the substrate as illustrated in Fig. 1 when oscillation light is to be taken from the substrate side. Hence, high-density arrayal is also difficult in this case.

[0012] Furthermore, in the device as illustrated in Fig. 2, the substrate is not a substrate of transparent material, and therefore light cannot be taken from the substrate side. Further, since an electrode wiring is formed for each light emitting portion at its stepped portion, the wiring process is difficult and its yield is degraded. Particularly, when the dielectric multi-layer mirror is to be formed on the semiconductor layer of the structure as illustrated in Fig. 2, the yield is drastically injured.

SUMMARY OF THE INVENTION

[0013] An object of the present invention is to provide a surface-type optical device whose growth substrate is removed over an area of plural active regions and which is suitable for a two-dimensional surface-type optical device of an array-type whose fabrication is simple and whose productivity is high, as to its fabrication method and a display apparatus using such a surface-type optical device.

[0014] A surface-type optical device for achieving the object of the present invention includes a first substrate, a plurality of active regions formed and disposed on the first substrate (growth substrate), and a control unit for injecting a current into or applying an inverse voltage to each active region. A portion of the first substrate is removed over an area including at least two active regions, and each active region is constructed such that light is output from or input into the active region perpendicularly to the first substrate. In this structure, hole-etching of the substrate is executed over the plural active regions (not for each active region), so that intervals between the active regions can be narrowed without considering interference between etched holes and even a high-density array can be readily produced with high productivity.

[0015] Based on the above fundamental structure, the following specific structures are possible, with the following technical advantages.

[0016] The active regions are arrayed, and a portion of the growth substrate is removed over an area of all the arrayed active regions. A desired number of the active regions are arranged in a two-dimensional array, for example, and the growth substrate is removed in the overall area. Therefore, even when the active regions are arrayed with a high degree of integration and high density, the hole-etching can be effected stably and accurately.

[0017] A portion of the growth substrate (e.g., a frame form) is left outside all the arrayed active regions. A process of the hole-etching can be readily conducted and a mechanical strength of the device can be secured, so the reliability can be improved.

[0018] The active regions are arrayed, and a portion of the substrate is left in a lattice-shaped form over an area of all the arrayed active regions. Adequate mechanical strength can be secured even if the growth substrate is not bonded to another substrate. Accordingly, its reliability can be improved with a simple structure.

[0019] The growth substrate with the active regions arrayed thereon is bonded to a second substrate with the active regions interposed between the growth substrate and the second substrate. Adequate mechanical strength can be secured by a simple process, and its reliability can be improved.

[0020] The control unit includes a common electrode common to the active regions formed on a remaining portion of the growth substrate. When the growth substrate is electrically conductive (typically, impurity-doped semiconductor), an electrode on the side of the epitaxially-grown layers can be simply formed on the remaining portion of the growth substrate as a common electrode.

[0021] The control unit includes an electrode wire pattern formed in the area including at least two active regions (an area where the growth substrate is removed) to take out each electrode from each active region. Thus, the active regions can be independently driven by such an electrode structure.

[0022] The first substrate with the active regions arrayed thereon is bonded to a second substrate with the active regions interposed between the first and second substrates, the control unit includes an electrode pattern formed on a surface of the active regions, to which the second substrate is bonded, and the electrode pattern is exposed by a removal of an outermost portion of the first substrate and a portion of the active regions to take out each electrode from each active region. Thus, the active regions can be independently driven similarly.

[0023] The first substrate with the active regions arrayed thereon is bonded to a second substrate with the active regions interposed between the first and second substrates, and the control unit includes an electrode pattern formed on a surface of the second substrate, to which the first substrate is bonded such

that the electrode pattern is electrically connected to each active region to take out each electrode from each active region. Thus, the active regions can be independently driven similarly.

[0024] The control unit includes positive and negative electrodes formed in a matrix form such that each active region can be driven independently. When the number of the arrayed active regions is large, the patterning will be too complicated if an independent driving of the respective pixels is conducted by the electrode patterning. In such a case, the matrix driving is advantageous.

[0025] The first substrate with the active regions arrayed thereon is bonded to a second substrate with the active regions interposed between the first and second substrates, and the second substrate is a semiconductor substrate with an electronic circuit formed thereon. Thus, an opto-electronic integrated circuit with an electronic circuit and a surface-type optical device can be readily formed on a common Si substrate, for example.

[0026] The active region includes a light emission layer such that a surface emitting device for emitting light perpendicularly to the first substrate is formed. A surface emitting device, such as a surface emitting semiconductor laser, can be thus formed. In this case, the surface emitting device may be a vertical cavity surface emitting laser with a pair of reflection mirrors provided on opposite sides of the light emission layer. Further, the surface emitting device may be a light emitting device with at most a reflection mirror provided on one side of the light emission layer.

[0027] The active region has a light absorptive layer such that a surface-type light receiving device for receiving light input perpendicularly to the first substrate is formed. In this case, the surface-type light receiving device may be a light receiving device with at least a reflection mirror provided on at least a side of the light reception layer. Input light can be effectively received by the light absorptive layer due to collection of light by the reflection mirror.

[0028] The active region includes at least a reflection mirror consisting of two kinds of dielectric layers (such as dielectric glass) which are alternately layered. A surface-type optical device can be thus formed at a relatively inexpensive cost.

[0029] The active region includes at least a reflection mirror consisting of two kinds of semiconductor layers which are alternately layered. In this case, the mirror can be fabricated successively to other epitaxial layers during a single process, so its fabrication process can be simplified.

[0030] The first substrate with the active regions arrayed thereon is bonded to a second substrate of a transparent material with the active regions interposed between the first and second substrates, each active region includes a light emission layer such that a surface emitting device for emitting light perpendicularly to the first substrate is formed, and a fluorescent sub-

stance is provided between the surface emitting device and the second substrate such that display can be performed by light of a color at an emission wavelength of the surface emitting device or light of a fluorescence color generated when the fluorescent substance is stimulated by the light from the surface emitting device. When a two-dimensional surface emitting device of an array type is formed and fluorescent substances of R (red), G (green) and B (blue) are provided for each emission point, an all-solid-state full-color display apparatus can be obtained with high productivity.

[0031] The active region includes layers of compound semiconductor consisting of a III-group element selected from B, Al, Ga and In and a V-group element, N, or an active layer of an oxide of Zn and clad layers of an oxide of Mg. Thus, a surface emitting device, such as a highly-efficient LD or LED, for emitting light from blue to ultraviolet can be fabricated, and a high-luminance full-color display apparatus can be provided.

[0032] The active region may preferably have a current constriction structure for constricting a current flow.

[0033] A fabrication method of a surface-type optical device for achieving the object of the present invention includes a step of epitaxially growing layers including an active layer on a first substrate, a step of forming a plurality of active regions on the first substrate, each of which is constructed such that light is output from or input into each active region perpendicularly to the first substrate, and a step of removing a portion of the first substrate over an area including at least two active regions. The removing step may be performed after or before the forming step.

[0034] A step of bonding a side of the epitaxially-grown layers of the first substrate to a second substrate may be further performed. The removing step may be performed after or before the bonding step.

[0035] A step of forming a current constriction structure for constricting a current flow to the active layer in the active region may be further performed.

[0036] A step of forming a reflection mirror on a side of the epitaxially-grown layers of the first substrate may be further performed.

[0037] A step of forming a reflection mirror on a face of the epitaxially-grown layers exposed by the removing step of the first substrate may be further performed.

[0038] The principle of the present invention will be described using an example (this is a first embodiment, described below).

[0039] A hole-etching of a growth substrate is performed only over a two-dimensional array area of light emission regions, after the growth substrate is bonded to another substrate, such as Si, as illustrated in Fig. 3A. Thus, the growth substrate is left, for example, in a frame shape in an area outside the area of the light emission regions. Intervals between the light emission regions (pixels) can hence be decreased, and a highly-dense integration of those pixels is made possible. In this case, an electrode can be taken from the side of the

growth substrate. Where no epitaxial mirror is provided on the substrate, a dielectric multi-layer mirror only needs to be formed after the etching of the growth substrate.

[0040] In the structure of this example, an essential element of the present invention only consists in that a plurality of active regions (such as light emission layers and light absorption layers) are arranged on a common growth substrate and that the growth substrate is partially removed only in a portion wherein at least two active regions are formed. Other specific structures are not essential to the present invention, but are only particular to this example.

[0041] The fabrication method of the example will be briefly described using Figs. 4A and 4B. As illustrated in Fig. 4A, a laser structure in the form of an active layer sandwiched between p-type and n-type clad layers is epitaxially grown on a semiconductor substrate of a single crystal, a region around the light emission region is etched into an annular shape, and the etched groove is buried with polyimide or the like. The light emission region is shaped into, for example, a cylinder with a diameter of 20 μm , and the etched annular shape has an outer diameter of 40 μm . Here, the periphery of the active layer is selectively wet-etched by several microns to be shaped into a circle with a diameter of about 15 μm , considering the effective diameter of a reflection mirror to be fabricated later. As illustrated in Fig. 4B, after an electrode is formed, the electrode and the semiconductor cap layer are etched into a circular shape of a diameter about equal to that of the active layer, and a dielectric multi-layer mirror is formed using a RF sputtering method or the like.

[0042] As illustrated in Fig. 4C, the substrate is polished to a thickness of about 100 μm , and an electrode is then formed on the bottom surface of the substrate and annealed. Thereafter, after the side of the dielectric mirror of the growth substrate is bonded to an InP substrate with its thermally-oxidized surface thereon, for example, the electrode and semiconductor substrate are removed except the frame-shaped portion. The bonding is conducted using an adhesive of a type which softens when heated, or a direct bonding with a solid-phase junction. The removal of the substrate is performed using wet etching, dry etching, or their combination.

[0043] As illustrated in Fig. 4D, a dielectric mirror is then formed only over the etched area of the growth substrate by using a lift-off method or the like, and the electrode on the side of the epitaxial layers is exposed by etching an outer portion of the frame-shaped substrate. Such a VCSEL array as illustrated in Fig. 3A can be fabricated.

[0044] Since those light emission regions can be arranged in a two-dimensional array on the original semiconductor substrate, a surface-emitting type array device can be readily fabricated. Regarding the etching of the semiconductor substrate, holes are not individu-

ally etched for the respective pixels differently from the prior art device, and instead the substrate is etched over the array area, so that no limitations is imposed on either the device intervals or the yield.

[0045] Further, the area of the device can be enlarged according to the present invention, compared to the case where the semiconductor mirror is directly bonded. The size of the device is generally limited by the size of the semiconductor substrate (about a 3-inch diameter in the case of compound semiconductor), but the size of the device can be further expanded by bonding the substrates to another support substrate. An independent electrode can be taken from each pixel on the growth substrate side, or electrodes on the support substrate side and the growth substrate side can be patterned in a matrix form as illustrated in Fig. 5 to attain the electrical conduction. Portions between the light emission regions (pixels) can be etched and polyimide can be put thereinto to prevent interference of current. Such an array laser can be applied to a two-dimensional array light source for use in optical information processing or optical interconnection. Further, such an array device can be formed of material capable of emitting blue or ultraviolet light, and such a device can be applied to a full-color display device in which fluorescent substances of R, G and B are deposited on a glass surface.

[0046] These advantages and others will be more readily understood in connection with the following detailed description of the preferred embodiments in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0047]

Fig. 1 is a perspective view with a cut-away portion illustrating the structure of a first prior art VCSEL array.

Fig. 2 is a cross-sectional view of a second prior art device.

Fig. 3A is a perspective view with a cut-away portion illustrating the structure of a VCSEL array of a first embodiment according to the present invention.

Fig. 3B is a cross-sectional view illustrating the structure of a single active region of the first embodiment.

Figs. 4A through 4D are respectively cross-sectional views illustrating fabrication steps of the first embodiment.

Fig. 5 is a perspective view with a cut-away portion illustrating the structure of a VCSEL array of a second embodiment according to the present invention.

Fig. 6 is a cross-sectional view illustrating the structure of a single VCSEL fabricated by using a solid-phase junction of a third embodiment according to the present invention.

Fig. 7 is a cross-sectional view illustrating the structure of a VCSEL (two VCSELs are depicted) fabricated by using an adhesive containing electrically-conductive particles of a fourth embodiment according to the present invention.

Fig. 8 is a cross-sectional view illustrating the structure of a single VCSEL with an epitaxial mirror of a fifth embodiment according to the present invention.

Fig. 9 is a perspective view illustrating the structure of a VCSEL array of a sixth embodiment according to the present invention.

Fig. 10 is a cross-sectional view illustrating the structure of a display apparatus using a VCSEL array of a seventh embodiment according to the present invention.

Fig. 11 is a cross-sectional view illustrating the structure, in which a VCSEL array and an electronic circuit are integrated, of an eighth embodiment according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

[0048] A first embodiment of the present invention is directed to a VCSEL array in which each VCSEL of an InGaAs/InGaAsP series with a 1.3- μ m wavelength band grown on a single crystal semiconductor substrate 1 of InP is bonded to a Si substrate 12 whose surface is insulated by thermal oxidization. Fig. 3A illustrates its overall perspective view with a cut-away portion, and Fig. 3B illustrates a detailed cross-sectional view of a light emitting region (or a pixel) of the VCSEL array.

[0049] In the first embodiment, an active layer 3 is sandwiched between n-type and p-type clad layers 2 and 4, and dielectric multi-layer mirrors 9 and 10 are provided at its opposite ends. The dielectric multi-layer mirror 9 is bonded to the Si substrate 12 by an adhesive 11. Patterning of an electrode 7 at the Si-substrate side is made such that a current can be independently injected into each pixel, as illustrated in Fig. 3A. After the thus-formed wafer is bonded to the Si substrate 12 and the semiconductor substrate 1 is etched into a frame-like shape, the substrate 1 and an epitaxially-grown layer 14 at the periphery of the frame are partially removed to expose the electrode 7. The patterned electrode 7 is thus taken out. An electrode 8 on the side of the semiconductor substrate 1 is taken out as a common electrode to each pixel since a portion of the electrically-conductive substrate 1 is left in such a frame-like shape as illustrated in Fig. 3A. In Fig. 3A, dielectric mirrors 9 and 10 are omitted for the convenience of simple understanding, a pixel 15 is depicted in the form of an outer periphery of the active layer 3, and a light emitting layer 16 represents the active layer 3 itself.

[0050] A fabrication process of the first embodiment

will be described with reference to Figs. 4A-4D.

[0051] Initially, as illustrated in Fig. 4A, an n-InGaAs contact or etching stop layer 20, the n-InP clad layer 2, the strained multi-quantum well active layer 3 of undoped InGaAs/InGaAsP, the p-InP clad layer 4 and a p-InGaAs contact layer 5 are grown on the n-InP substrate 1 in the named order using a chemical beam epitaxy (CBE) method or the like. Layers down to the active layer 3 around the light emitting region are perpendicularly etched in an annular shape with an inner diameter of 20 μ m and an outer diameter of 40 μ m, using a reactive ion beam etching (RIE) method or the like.

[0052] Then, the side end of the InGaAs contact layer 5 is covered with a resist, and only the side end of the active layer 3 is etched several microns by a selective wet etching, so that the active layer 3 is thinned into a circular shape with a diameter of about 15 μ m. The diameter of the active layer 3 is thus made approximately equal to the effective diameter of the dielectric multi-layer (described later) to constrict the injected current to a necessary degree. The oscillation operation can hence be made efficient and preferable. When a mixture of sulfuric acid, hydrogen peroxide water and water (in the ratio of 3:1:1) is used as etchant, the InP clad layers 2 and 4 are not etched at all and the active layer 3, solely, is etched completely (thus, highly selective etching is achieved).

[0053] Further, there is a face-orientation dependency during the etching, so that when a (100) substrate is used, (010) face, (001) face and their inversely-oriented faces appear to form the active layer 3 of an approximately square shape. In this case, the anisotropy of gain occurs in the active layer 3, and polarization of the oscillation light is stabilized. Accordingly, the problem of kinks and the like due to a polarization instability of oscillation light in a conventional VCSEL can be solved. The thus-formed groove is buried with a polyimide 13 or the like.

[0054] Then, as illustrated in Fig. 4B, insulation is secured at the outer periphery of each pixel by forming a SiN layer 6 around the pixel. The p-side electrode 7 is formed by the patterning and deposition of Cr (its thickness: 500Å)/Au (its thickness: 5000Å). Within the pixel, circular portions of the electrode 7 and the contact layer 5 slightly larger than the active layer 3 are removed. Thereafter, the dielectric multi-layer 9 consisting of six pairs of Si/Al₂O₃ with a common thickness of $\lambda/4$ (λ : a real wavelength in the layer of the oscillation wavelength) is formed using an RF sputtering method or the like. In this step, annealing of the electrode 7 is conducted to obtain the electrode contact.

[0055] Then, after the InP substrate 1 is polished to a thickness of 100 μ m (the thickness as illustrated in Fig. 3A), the n-side electrode 8 of AuGe (its thickness: 2000Å)/Au (its thickness: 3000Å) is vacuum-evaporated and annealed to establish the electrode contact. Patterning is performed to leave an outer portion of the array region in the frame shape as illustrated in Fig. 3A.

and only a portion of the electrode 8 in the region for hole-etching is removed.

[0056] As illustrated in Fig. 4C, the dielectric multi-layer 9 is bonded to the thermally-oxidized Si substrate 12 with the adhesive 11, and the hole-etching of the substrate 1 is executed using chloric acid. The InGaAs contact or etching stop layer 20 is thus exposed. Since InGaAs cannot be etched by the chloric acid, the etching is completely stopped at the etching stop layer 20. The above bonding is performed by inserting a sheet of polyimide series between the multi-layer 9 and the substrate 12 and heating it to 200 °C.

[0057] Finally, as illustrated in Fig. 4D, the etching stop layer 20 is removed using an etchant of sulfuric acid series, and the dielectric multi-layer 10 consisting of six pairs of Si/Al₂O₃ is formed in the region of the VCSEL array only, using an RF sputtering method or the like. No multi-layer is formed on the frame for taking out the electrode 8. The outer periphery of the epitaxial layer 14 is etched and removed to take out the bonding-side electrode 7. The structure illustrated in Fig. 3A is thus completed.

[0058] When a multiplicity of the thus-formed pixels 15 are arranged on a semiconductor substrate, a high-density two-dimensional array laser with a low threshold can be readily fabricated. The 3x4 array of twelve pixels is illustrated in Fig. 3A, but the number can be increased. Further, when pixels are fabricated on each semiconductor substrate and the thus-formed substrates are bonded to another substrate in an appropriate arrangement, the number of the arrayed pixels can be further increased. In the first embodiment, each pixel can operate in a good condition even with the pixel interval of 100 μm.

[0059] Although the substrate 1 of the first embodiment is shaped into a frame as illustrated in Fig. 3A, only one side or a part of one side of the frame may be left in place of the entire frame, provided that there exists a remaining region for establishing a contact with the electrode 8.

[0060] Such a two-dimensional array laser can be used as a light source for high-speed parallel information transmission, optical interconnection and optical information processing.

[0061] In the first embodiment, the structure of the InGaAsP/InP series is formed on the InP substrate, but the choice of material series is not limited thereto, and the structure can be built in another wavelength band. The present invention can also be applied to the AlGaIn/InGaIn series on a sapphire substrate, and the InGaAlP/InAlP, InGaAs/AlGaAs and InGaInAs/AlGaAs(GaInP) series on a GaAs substrate. Especially, a 1.3-μm band laser constructed with the InGaInAs/AlGaAs(GaInP) series is superior in temperature characteristics and differential gain, so that the laser can operate without any temperature control. Here, when no heat sink is used and the above-discussed another substrate is transparent, oscillation light

can be taken from both upper and lower sides.

Second Embodiment

[0062] A second embodiment is directed to a VCSEL array in which an electrode 31 is also formed in a hole-etched surface as illustrated in Fig. 5 to effect a matrix driving. For this purpose, stripes of the electrode 7 extend in a column direction, while stripes of the electrode 31 extend in a row direction perpendicular to the column direction. In Fig. 5, the same members as those in Fig. 3A are designated by the same reference numerals.

[0063] The first half of the process of the fabrication of the second embodiment is similar to that of the first embodiment. The fabrication is similarly conducted up to the process of Fig. 4C except for the formation of the electrode 8 on bottom surface. The etching stop layer 20 is not removed and is instead used as the contact layer. In the process of Fig. 4C, a process similar to the surface process of Fig. 4B is performed. That is, a SiN layer is formed to secure the insulation of the periphery of each pixel, and an n-side electrode 31 of AuGe (its thickness: 2000Å)/Au (its thickness: 3000Å) is formed in a pattern as illustrated in Fig. 5. Circular portions of the electrode 31 and contact layer 20 of a 15-μm diameter are removed in each pixel 15, and a dielectric mirror is formed over the entire array region during the process of Fig. 4D (this mirror is not shown in Fig. 5).

[0064] Further, the epitaxial layer 14 can be removed in a cross-striped pattern and the thus-formed groove can be buried with polyimide or the like as illustrated in Fig. 5 to prevent interference of the n-side electrode. This process is executed before the formation of the SiN layer and the n-side electrode 31.

[0065] When the number of arrayed pixels is large, the patterning will be considerably complicated if the structure is built such that each pixel is driven with the electrode patterning similar to the first embodiment. Therefore, the matrix driving of the second embodiment is often more advantageous. Further, since a current is caused to flow through a thin layer, such as the clad layer 2, in an in-surface direction in the case of the common electrode of the first embodiment, the resistance may be high and high-frequency characteristic may be poor. The second embodiment can solve those problems.

Third Embodiment

[0066] In a third embodiment of the present invention, each pixel 15 as shown in Fig. 6 is formed after the wafer is bonded to the substrate 12 (in Fig. 6, the same members as those in Fig. 3B are designated by the same reference numerals). The materials to be used are the same as those of the above embodiments, and a VCSEL of an oscillation wavelength of 1.55 μm is constructed with the InGaAsP/InP series on an InP sub-

strate.

[0067] Similarly to the first embodiment, a substrate to be bonded is the Si substrate 12 with little loss at 1.55 μm whose opposite faces are polished. The final layer of the dielectric mirror 9 is made of Si, and the surface of the Si substrate 12 is directly bonded to sputtered amorphous Si at a heated temperature of 200 °C and with a load applied thereto. Thus, direct bonding is effected without any adhesive.

[0068] Here, if the pixel is fabricated beforehand, the bonding to the Si substrate 12 will be difficult owing to the surface unevenness and the influence of the polyimide 13. Therefore, it is desirable to perform the pixel-forming process after the bonding. The process may be done at higher temperatures to increase the bonding strength. Further, if the overall surface is caused to act as a junction surface, the surface is likely to be separated due to stress and so forth. Therefore, it is effective that the dielectric mirror 9 is only formed over a region with a certain area (about a 50- μm diameter in this embodiment) as illustrated in Fig. 6 and that the non-bonded surface without the mirror 9 is caused to act as a relaxation layer. A non-bonded region 41 is a vacant space, so an ambient gas during the bonding process can be introduced within the region 41. When the ambient gas has a negative pressure, a stable bonding state can be maintained. Heat radiation characteristic of the device is superior due to the direct bonding without any adhesive.

[0069] The fabrication method and structure of the third embodiment will be described with reference to Fig. 6.

[0070] Similarly to the first embodiment, the laser structure is epitaxially grown on the InP substrate (the structure of the active layer 3 is different from that of the first embodiment). After the insulation structure of the SiN 6 is formed, the electrode wiring pattern 7 of Ti (its thickness: 500Å)/Pt (its thickness: 1000Å)/Au (its thickness: 3000Å) is formed as a non-alloy electrode on the InGaAs contact layer 5. No diffusion occurs in the electrode 7 at the time of heating. Then, circular portions of the electrode 7 and the contact layer 5 are removed with such a diameter (here, 30 μm Ø, though depicted a little smaller in Fig. 6) as causes an effective diameter of the multi-layer mirror 9 to have a sufficient amount relative to that of the active layer 3. The multi-layer mirror 9 (whose final layer is Si) of Si/Al₂O₃ is deposited with a diameter of 50 μm by a lift-off method or the like.

[0071] The Si substrate 12 is then bonded as described above. Thereafter, after the InP substrate is removed similarly to the first embodiment, the formation process of the pixel is executed. The electrode 8 is formed in such an electrode pattern as illustrated in Fig. 5, so that the pixels 15 can be driven independently from each other. In Fig. 6, reference numeral 42 designates an etching stop or contact layer.

[0072] When the device is operated, light may be taken out from the side of the Si substrate 12, or from

the side where no Si substrate 12 is bonded as a heat sink.

[0073] In the third embodiment, the optical device and an integrated circuit fabricated on the Si substrate 12 can be provided on a common substrate, and hence an opto-electronic integrated device can be constructed at a relatively inexpensive cost. The optical device can be readily positioned even in a narrow location since no adhesive is used.

[0074] An example of such an opto-electronic integrated device is illustrated in Fig. 11. Fig. 11 depicts an integration portion between the pixel (surface emitting laser) array and a bipolar transistor 210 for driving the surface emitting laser, which transistor is formed at a final stage of the integrated circuit formed on a Si substrate 112. A dielectric mirror 109 is directly bonded, in a solid phase, to a SiN_x layer 200 which is a protective layer for a bare chip of Si devices. The solid-phase bonding between Si's is executed in the above-discussed fabrication process, but the bonding between Si and the SiN_x layer is similarly possible. Only a portion of the SiN_x layer 200 on a surface layer of the Si bare chip in a region, which is to be bonded to the surface emitting laser, may be removed, and the bonding may be performed to such a revealed surface of the Si substrate 112. It should be noted that the process temperature would not be raised too much when the bonding to a Si substrate with an integrated circuit thereon is performed.

[0075] In the bonding process, a laser electrode 107 and a collector electrode 201 of the transistor 210 are aligned with each other, and the driving transistor 210 is thus connected to each surface emitting laser. The transistor 210 is an npn-type in which the electrode 201 formed on an n-diffusion region 206 is a collector, an electrode 203 formed on a p-diffusion region 208 is a base and an electrode 202 formed on an n-diffusion region 207 is an emitter.

[0076] In Fig. 11, reference numeral 204 designates an n-diffusion region initially formed on the substrate 112, and reference numeral 205 designates a p-diffusion region for separating devices from each other. Further, reference numeral 101 designates a growth substrate, reference numeral 102 designates an n-clad layer, reference numeral 103 designates an undoped active layer, reference numeral 104 designates a p-clad layer, reference numeral 106 designates an insulating layer, reference numeral 108 designates an n-side electrode, reference numeral 110 designates a dielectric mirror, reference numeral 113 designates polyimide put in a groove portion, and reference numeral 132 designates polyimide put in another groove portion for preventing interference between the n-side electrodes 108.

[0077] The electrodes of the transistor other than the collector electrode 201 are connected to a CMOS circuit or the like formed on the Si substrate 112 through electric wires. The other electrode 108 of the surface emitting laser is also connected to a power source or the like

through a wire pattern formed on the substrate.

Fourth Embodiment

[0078] In a fourth embodiment of the present invention, an electrode pattern, which is formed on the side of the epitaxial layers in the above embodiments, is formed on the substrate to be bonded, and the electrode pattern is bonded and electrically connected to an electrode pad in a simple shape formed at each pixel.

[0079] In the structure as illustrated in Fig. 7 (in Fig. 7, the same portions as those in Fig. 6 are designated by the same reference numerals), Au 51 is deposited on the side of the pixel such that electrical conduction can be established between an upper portion of the dielectric mirror 9 and the electrode contact 7 of the pixel. Electrical conduction between the Au 51 on the upper portion of the dielectric mirror 9 and an electrode pattern 52 on the side of a substrate 55 is attained by a polyimide-series adhesive 54 containing electrically-conductive particles 53. The adhesive 54 has characteristics that electrical conduction can be achieved only between the electrode pads 51 and 52 while no conduction is established between recesses of stepped portions on both lateral sides of the electrode pads 51 and 52.

[0080] The wiring pattern is formed of a plating 52 of Cu/Ni/Au with a thickness of about 15 μm on the resin substrate 55. After the alignment between the electrode pads 51 and 52 is effected by using infrared transmitting light, the bonding thereof is conducted by heating it to 200 $^{\circ}\text{C}$ while applying a load thereto. The dielectric mirror 9 has a diameter of 50 μm similarly to the third embodiment, and its height is 2 μm . As illustrated in Fig. 7, the conductive particles 53 are inserted between the two electrode pads 51 and 52 and the electrical conduction is secured therebetween, while no electrical conduction is attained in regions without any pad since those particles 53 are not connected to each other therein. Vacant portions on the bonding side are filled with the polyimide adhesive 54.

[0081] The pixel is formed similarly to the third embodiment. Regarding the structure of the VCSEL in Fig. 7, the growth substrate is removed and the pixels are fabricated after the bonding step, similarly to the third embodiment. The pixel, however, may be fabricated prior to the bonding step as in the first embodiment. Further, the electrode wiring pattern is the same as that in Fig. 3A or Fig. 5.

[0082] In the fourth embodiment, since only the required portions can be electrically connected readily and positively, this embodiment can be especially effectively used where the wiring pattern is more complicated and denser than that in the above embodiments. Further, heat radiation characteristics of the device of the fourth embodiment are better than those of the first embodiment since the adhesive containing the conductive particles is used.

[0083] So-called anisotropic electrically-conductive adhesive, in which conductive particles are thinly diffused, is used in the fourth embodiment, but any bonding method may be used, provided that electrical contact can be effected only between the desired electrodes while insulation is secured between other electrode wires.

[0084] As other bonding methods, there exists a method in which solder, Ag paste or the like is selectively placed only at regions whereat electrical contact is desired, as well as a method in which electrode metals are pressed to each other by applying a load to the substrate, and so forth. As the selective solder formation, there exists a so-called flip-chip packaging in which a solder ball is placed, and a method in which a film of solder is selectively formed by plating. As the selective formation of Ag paste, there exist a screen printing method and the like. In either method, selective formation is possible in a size of about 50- μm square.

[0085] Further, though the resin substrate 55 is used as the substrate to be bonded, it is naturally possible to connect a bare chip to another bare chip of the Si substrate on which the integrated circuit is formed as in the third embodiment, as illustrated in Fig. 12.

Fifth Embodiment

[0086] In the above embodiments, InP series and dielectric mirrors are used, but in a fifth embodiment, the concept of the present invention is applied to a VCSEL of GaAs series provided with epitaxial mirrors. When the GaAs substrate is used, high-reflection DBR mirrors can be formed at opposite end surfaces by epitaxially growing AlAs/GaAs (or AlGaAs) multi-layers together with the active layer. Therefore, no separate formation step of the dielectric mirror is needed, so that the overall process can be considerably simplified.

[0087] Fig. 8 illustrates such a structure. An n-AlAs/AlGaAs (twenty-five pairs) DBR mirror 61, a GaAs/AlGaAs multiple quantum well active layer 62 sandwiched between AlGaAs spacers, and a p-AlAs/AlGaAs (thirty pairs) DBR mirror 63 are formed on the n-GaAs substrate (not shown) during a single epitaxial growth process. The overall thickness of the active layer and the spacer layers is set to one wavelength of the oscillation wavelength. In this embodiment, the oscillation wavelength is 835 nm, and that overall thickness is about 250 nm. The uppermost layer of the p-DBR mirror 63 is made of GaAs such that the electrode contact to the mirror 63 can be improved. Also in this embodiment, the pixel is formed similarly to the first embodiment, but only the formation of the insulation structure of the SiN 6, the burying with the polyimide 13, and the formation of the p-electrode pattern 7 are needed since the two mirrors has already formed.

[0088] After this wafer is bonded to the Si substrate 12 or the like, the n-GaAs substrate is removed except a portion thereof, as in the above embodiments. Here,

selective etching of the GaAs substrate and the first layer AlAs of the n-DBR mirror 61 is conducted using a wet etching of ammonia plus hydrogen peroxide series and dry etching, for example. The n-side electrode may be the same as that of the first embodiment.

[0089] There is no need to remove the n-GaAs substrate where light is taken from the side of the p-DBR mirror 63, but in such a case, precise and accurate patterning is required to form a window for taking out the light in the p-side electrode 7. Therefore, where the device is a GaAs-series device whose wavelength band (below about 850 nm) is absorbable by the growth substrate, the fifth embodiment is effective since no window is formed in the p-electrode 7 and the n-GaAs substrate is removed.

Sixth Embodiment

[0090] In a sixth embodiment, layers grown on the growth substrate are not bonded to another substrate, and a multiplicity of regions with small areas, where active regions are highly densely arrayed, are arranged, as illustrated in Fig. 9. When the hole-etching region has a small area, say about 300- μm square (this value is roughly determined by the strength needed to maintain the laser substrate and a desired value of electric resistance on the side of an electrode 78), a lattice-shaped substrate 71 has a sufficient strength and hence no bonding to another substrate is needed. In this embodiment, four (2x2) pixels 15 are integrated at a pitch of 125 μm in the area of 300 μm^2 , the lattice-shaped substrate has a width of 100 μm , and sixteen partitions each including four pixels are arranged in a two-dimensional pattern.

[0091] Where the integration degree is low (i.e., the pitch between pixels is relatively large), the structure of this embodiment formed by a simple process is effective since the lattice-shaped substrate 71 with the electrode 78 thereon can be left between the pixels 15.

Seventh Embodiment

[0092] In a seventh embodiment, lasers or LEDs of GaN-series material for emitting light from blue to ultraviolet (wavelength: 420 nm~380 nm) are bonded to another substrate to form the arrangement in a two-dimensional array, as described in the above embodiments. When a glass is used as that another substrate and fluorescent substance is applied to a glass substrate 92 for each pixel as illustrated in Fig. 10 such that fluorescent light of R, G or B can be emitted therefrom, the device can be used as a full-color display device by using optical stimulation by the light from blue to ultraviolet.

[0093] The pixels can be formed with the pixel diameter of 25 μm and the interval of about 75 μm , and the area of the arrayed pixels can be largely increased. Therefore, even a panel-type large-scale full-color display device can be built.

Since a low-threshold laser is used as the light emitting source, display can be performed with small consumption electric power and large luminance, and no high voltage and no vacuum are needed.

[0094] The structure and process are similar to those of the above embodiments. Those will be described with reference to Fig. 10.

[0095] A low-temperature buffer layer (not shown) of GaN or AlN, which can be formed at low growth temperature, is formed with a relatively large thickness of about 10 μm on a sapphire substrate (not shown). A clad layer 81 of n-GaN/n-AlGaIn, a multiple quantum well active layer 82 of undoped InGaIn/AlGaIn, a clad layer 84 of p-AlGaIn/p-GaN, and a p-GaN cap layer 85 are then grown using a metal organic vapor phase epitaxy (MOVPE) method or the like. Similarly to the first embodiment, the pixel and the like are formed using etching, such as RIBE, and so forth. In this embodiment, selective constriction etching of the active layer 82 is difficult, so a current block region 83 is formed by selectively oxidizing the AlGaIn layer (a barrier layer) in the active layer 82. This process uses the phenomenon that when heating process is performed at about 500 °C in the atmosphere of water vapor, an oxidized portion proceeds inwardly from a side wall of the layer containing easily-oxidizable Al. At this time, the side wall of AlGaIn layer in the clad layer 84 is also oxidized similarly, but no current block region is formed thereat since the cap layer 85 remains unchanged due to its GaN. Therefore, no problem occurs. Then, after the groove portion is buried with a burying layer 94, Ni (its thickness: 1000 Å)/Au (its thickness: 3000 Å) is deposited as a p-side electrode 87. Reference numeral 86 designates an insulating layer.

[0096] Thereafter, a dielectric multi-layer mirror 89 of eighteen pairs of SiO₂/MgO is formed using RF sputtering method or the like, and the thus-formed wafer is bonded to the glass substrate 92 on which RGB fluorescence substance 93 is patterned corresponding to each pixel, by adhesive 91.

[0097] The sapphire substrate is removed, except for its outer frame portion, by polishing or the like until the buffer layer appears. The exposed low-temperature buffer layer of GaN or AlN is removed by etching, using phosphoric acid heated up to 300 °C. Here, the etching rate of the n-GaN layer in the clad layer 81 of epitaxially-grown single crystal n-GaN/n-AlGaIn is very slow for the above etchant, and hence the selective etching can be effected.

[0098] A matrix-shaped wiring is formed similarly to the second embodiment. Specifically, a pattern of Ti (its thickness: 500 Å)/Al (its thickness: 1 μm)/Au (its thickness: 2000 Å) is formed as an n-side electrode 95, as illustrated in Fig. 5. The epitaxial layers may be removed in the lattice-shaped pattern 32 and polyimide or the like may be put therein, as illustrated in Fig. 5, so that the interference of the n-side electrode can be prevented.

Finally, after the electrode 95 in the pixel is removed in a circular shape of 15- μ m diameter, a dielectric multi-layer mirror 90 of SiO_2/MgO is laid down over all the array region (not on the outer frame portion of the growth substrate). The display can be thus performed by the matrix driving.

[0099] In the case of the LED, no dielectric mirror 89 is formed on the side of the fluorescent substrate 93. Also in the first to sixth embodiments, the LED array can be formed without forming the mirror on the light-takeout side. Thus the LED can be fabricated readily.

[0100] In the above embodiments, light emission devices are arranged, but the light emission device can be replaced by a light receiving device. Where the electric wire and so forth are formed on the bonding substrate and light need be input from the side of the growth substrate not of the bonding substrate, the array of the light receiving devices can be relatively readily formed when the growth substrate is removed as illustrated in Fig. 3A. The structure in this case may be approximately the same as that of Figs. 3A and 3B, except that the active layer is an absorptive layer and an inverse electric field is applied across the electrodes to take a photocurrent therefrom. When the device is constructed as light receiving device, no multi-layer mirrors is basically needed, but its light reception efficiency can be improved if the mirror on the side of the bonding substrate is formed, similarly to the laser, to reflect light thereat and return it to the light absorptive layer.

[0101] As described in the foregoing, according to the present invention, a surface-type optical device capable of being readily fabricated with good productivity and suitable for a two-dimensional array light emission apparatus can be achieved. Its preferable fabrication method, display apparatus using that device and the like can also be obtained.

[0102] Except as otherwise disclosed herein, the various components shown in outline or block form in any of Figures 1-11 are individually well known in the optical semiconductor device, and their internal construction and operation are not described herein.

[0103] While the present invention has been described with respect to what are presently considered to be the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. The present invention is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

[0104] A surface-type optical device, such as a surface emitting laser device, includes a first substrate, a plurality of active regions formed and disposed on the first substrate, and a control unit for injecting a current into or applying an inverse voltage to each active region. A portion of the first substrate is removed over an area including at least two active regions. The active region is constructed such that light is output from or input into each active region perpendicularly to the first substrate.

A second substrate may be bonded to a side of the epitaxially-grown layers of the first substrate.

Claims

1. A surface-type optical device comprising:

a first substrate;
a plurality of active regions formed and disposed on said first substrate, a portion of said first substrate being removed over an area including at least two said active regions; and
control means for injecting a current into or applying an inverse voltage to each of said active regions, light being output from or input into each of said active regions perpendicularly to said first substrate.

2. A surface-type optical device according to claim 1, said active regions being arrayed, and a portion of said first substrate being removed over an area of all of said arrayed active regions.
3. A surface-type optical device according to claim 2, a portion of said first substrate being left outside all of said arrayed active regions.
4. A surface-type optical device according to claim 1, said active regions being arrayed, and a portion of said first substrate being left in a lattice-shaped form over an area of all of said arrayed active regions.
5. A surface-type optical device according to any one of claims 1 to 4, further comprising a second substrate, said first substrate having said active regions arrayed thereon and being bonded to said second substrate with said active regions interposed between said first substrate and said second substrate.
6. A surface-type optical device according to any one of claims 1 to 5, said control means including a common electrode common to said active regions formed on a remaining portion of said first substrate.
7. A surface-type optical device according to any one of claims 1 to 6, said control means including an electrode pattern formed in said area including at least two active regions to take out each electrode from each of said active regions.
8. A surface-type optical device according to any one of claims 1 to 7, further comprising a second substrate, said first substrate with said active regions arrayed thereon being bonded to said second sub-

strate with said active regions interposed between said first substrate and said second substrate, and said control means including an electrode pattern formed on a surface of said active regions, to which said second substrate is bonded, said electrode pattern being exposed by a removal of an outermost portion of said first substrate and a portion of said active regions to take out each electrode from each of said active regions.

9. A surface-type optical device according to any one of claims 1 to 7, further comprising a second substrate, said first substrate with said active regions arrayed thereon being bonded to said second substrate with said active regions interposed between said first substrate and said second substrate, and said control means including an electrode pattern formed on a surface of said second substrate, to which said first substrate is bonded such that the electrode pattern is electrically connected to each of said active regions to take out each electrode from each of said active regions.
10. A surface-type optical device according to any one of claims 1 to 5, said control means comprising positive and negative electrodes formed in a matrix form such that each of said active regions can be driven independently.
11. A surface-type optical device according to any one of claims 1 to 6, further comprising a second substrate, said first substrate with said active regions arrayed thereon being bonded to said second substrate with said active regions interposed between said first substrate and said second substrate, and said second substrate comprising a semiconductor substrate with an electronic circuit formed thereon, at least one electrode of said electronic circuit being electrically connected to each of said active regions through an electric wire formed on said second substrate.
12. A surface-type optical device according to any one of claims 1 to 11, said active region comprising a light emission layer such that a surface emitting device for emitting light perpendicularly to said first substrate is formed.
13. A surface-type optical device according to claim 12, said surface emitting device comprising a vertical cavity surface emitting laser with a pair of reflection mirrors provided on opposite sides of said light emission layer.
14. A surface-type optical device according to claim 12, said surface emitting device comprising a light emitting device with at most a reflection mirror provided on one side of said light emission layer.

15. A surface-type optical device according to any one of claims 1 to 11, said active region comprising a light absorptive layer such that a surface-type light receiving device for receiving light input perpendicularly to said first substrate is formed.

16. A surface-type optical device according to claim 15, said surface-type light receiving device comprising a light receiving device with at least a reflection mirror provided on at least a side of said light reception layer.
17. A surface-type optical device according to any one of claims 1 to 16, said active region comprising at least a reflection mirror consisting of two kinds of dielectric layers which are alternately layered.
18. A surface-type optical device according to any one of claims 1 to 16, said active region comprising at least a reflection mirror consisting of two kinds of semiconductor layers which are alternately layered.
19. A surface-type optical device according to any one of claims 1 to 14, 17 and 18, further comprising a second substrate of a transparent material, said first substrate having said active regions arrayed thereon and being bonded to said second substrate with said active regions interposed between said first substrate and said second substrate, each of said active regions comprising a light emission layer such that a surface emitting device for emitting light perpendicularly to said first substrate is formed, and further comprising a fluorescent substance provided between said surface emitting device and said second substrate such that display can be performed by light of a color at an emission wavelength of said surface emitting device or light of a fluorescence color generated when said fluorescent substance is stimulated by the light from said surface emitting device.
20. A surface-type optical device according to any one of claims 1 to 19, said active regions comprising layers of compound semiconductor consisting of a III-group element selected from the group consisting of B, Al, Ga and In and N.
21. A surface-type optical device according to any one of claims 1 to 19, said active regions comprising an active layer of an oxide of Zn and clad layers of an oxide of Mg.
22. A surface-type optical device according to any one of claims 1 to 21, said active regions including a current constriction structure for constricting a current flow.
23. A fabrication method of a surface-type optical

device, comprising the steps of:

epitaxially growing layers including an active layer on a first substrate;
forming a plurality of active regions on the first substrate, each active region being constructed such that light is output from or input into each active region perpendicularly to the first substrate; and
removing a portion of the first substrate over an area including at least two of the active regions.

24. A fabrication method according to claim 23, further comprising the step of bonding a side of the epitaxially-grown layers of the first substrate to a second substrate.
25. A fabrication method according to claim 23 or claim 24, further comprising the step of forming a current constriction structure for constricting a current flow to the active layer in the active region.
26. A fabrication method according to any one of claims 23 to 24, further comprising the step of forming a reflection mirror on a side of the epitaxially-grown layers of the first substrate.
27. A fabrication method according to any one of claims 23 to 24, further comprising the step of forming a reflection mirror on a face of the epitaxially-grown layers exposed by said removing step.
28. A fabrication method according to any one of claims 23 to 27, said removing step being performed after said forming step of the active regions.
29. A fabrication method according to any one of claims 23 to 27, said forming step of the active regions being performed after said removing step.
30. A fabrication method according to any one of claims 24 to 29, said removing step being performed after said bonding step.

FIG.1
PRIOR ART

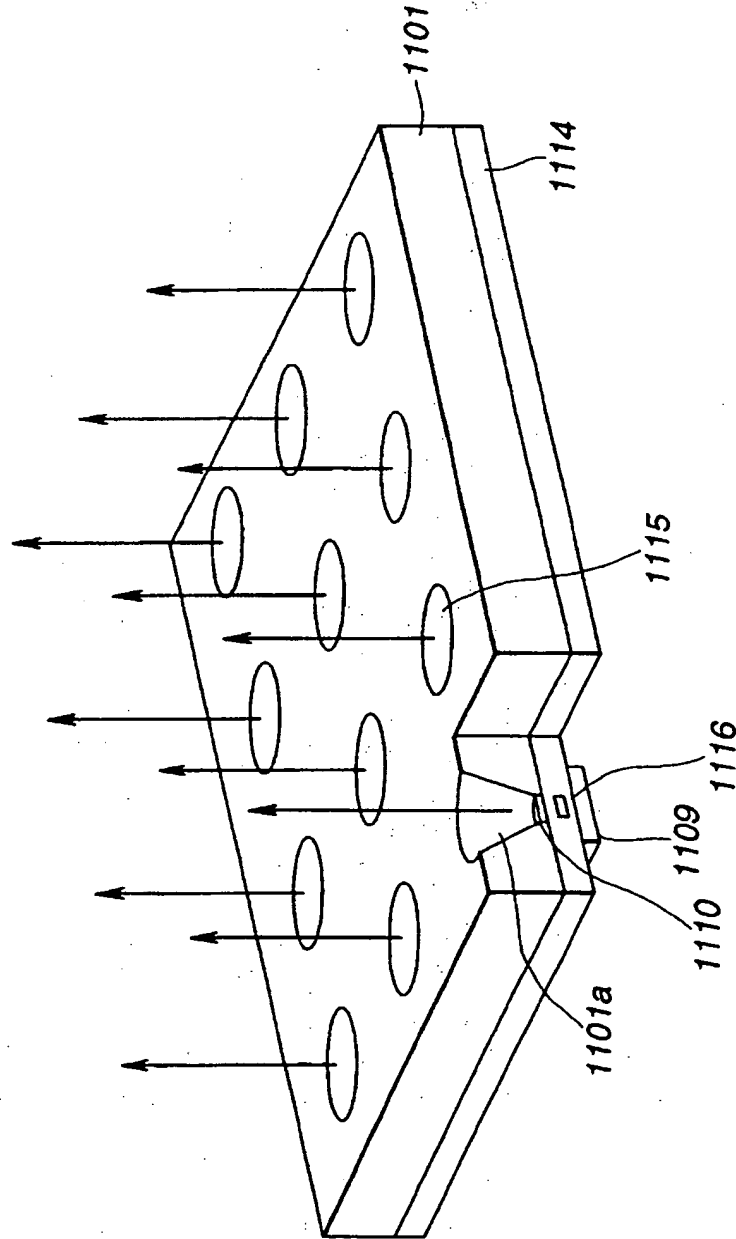


FIG.2
PRIOR ART

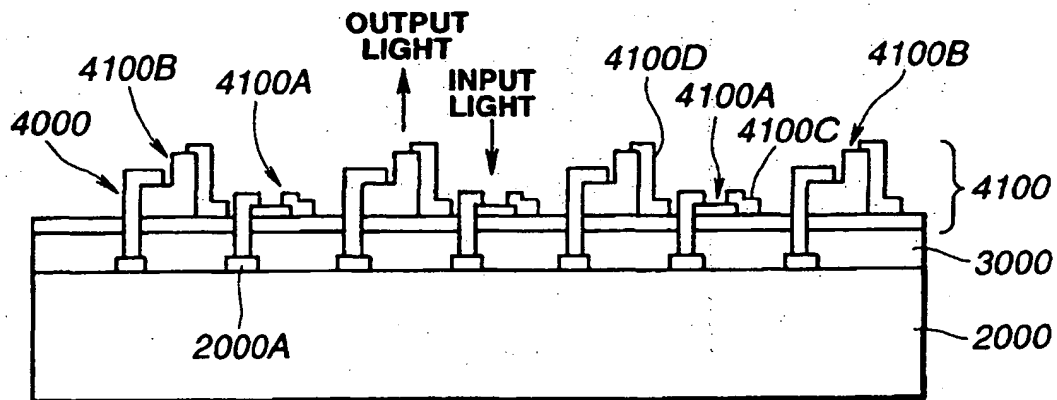


FIG.3A

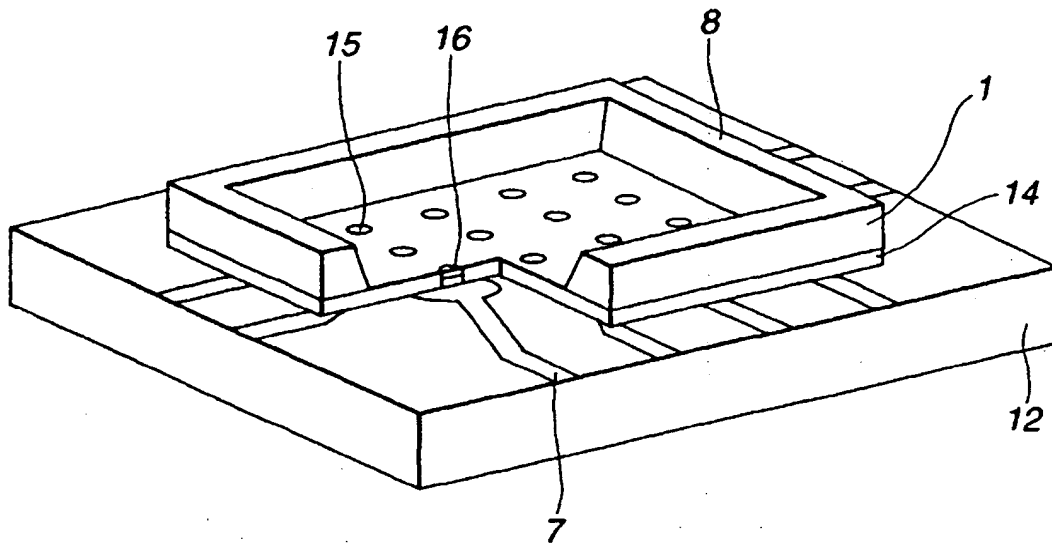


FIG.3B

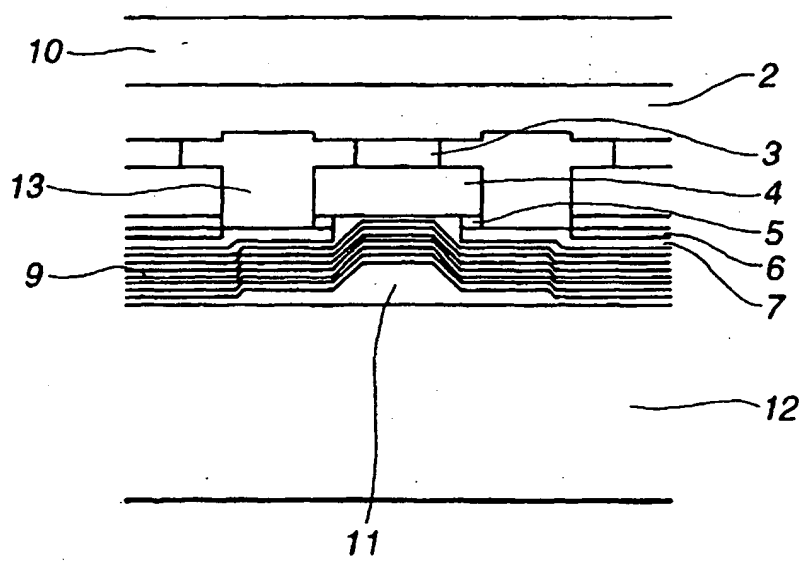


FIG.4A

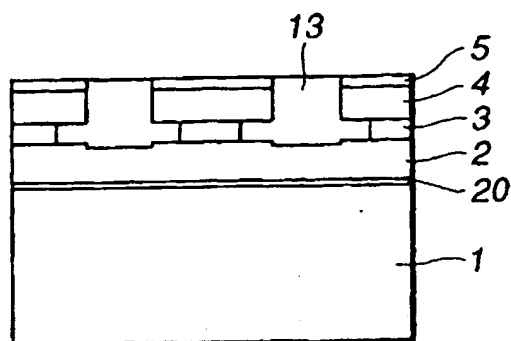


FIG.4B

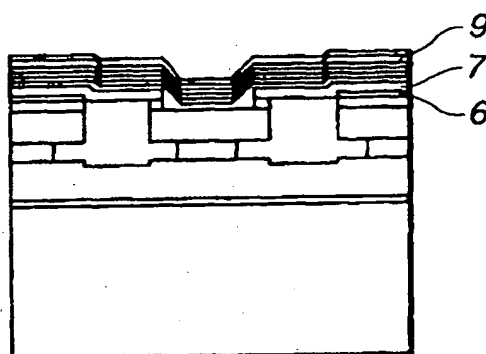


FIG.4C

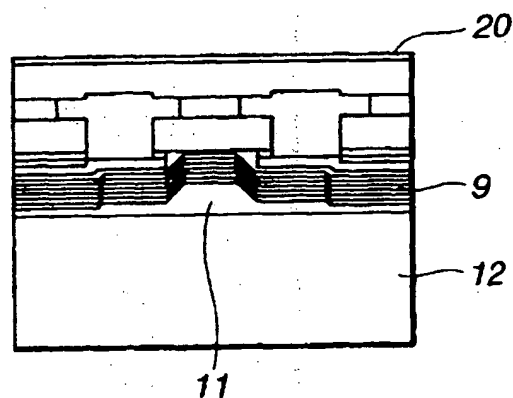


FIG.4D

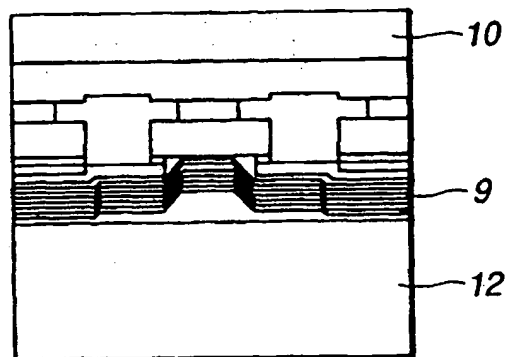


FIG.5

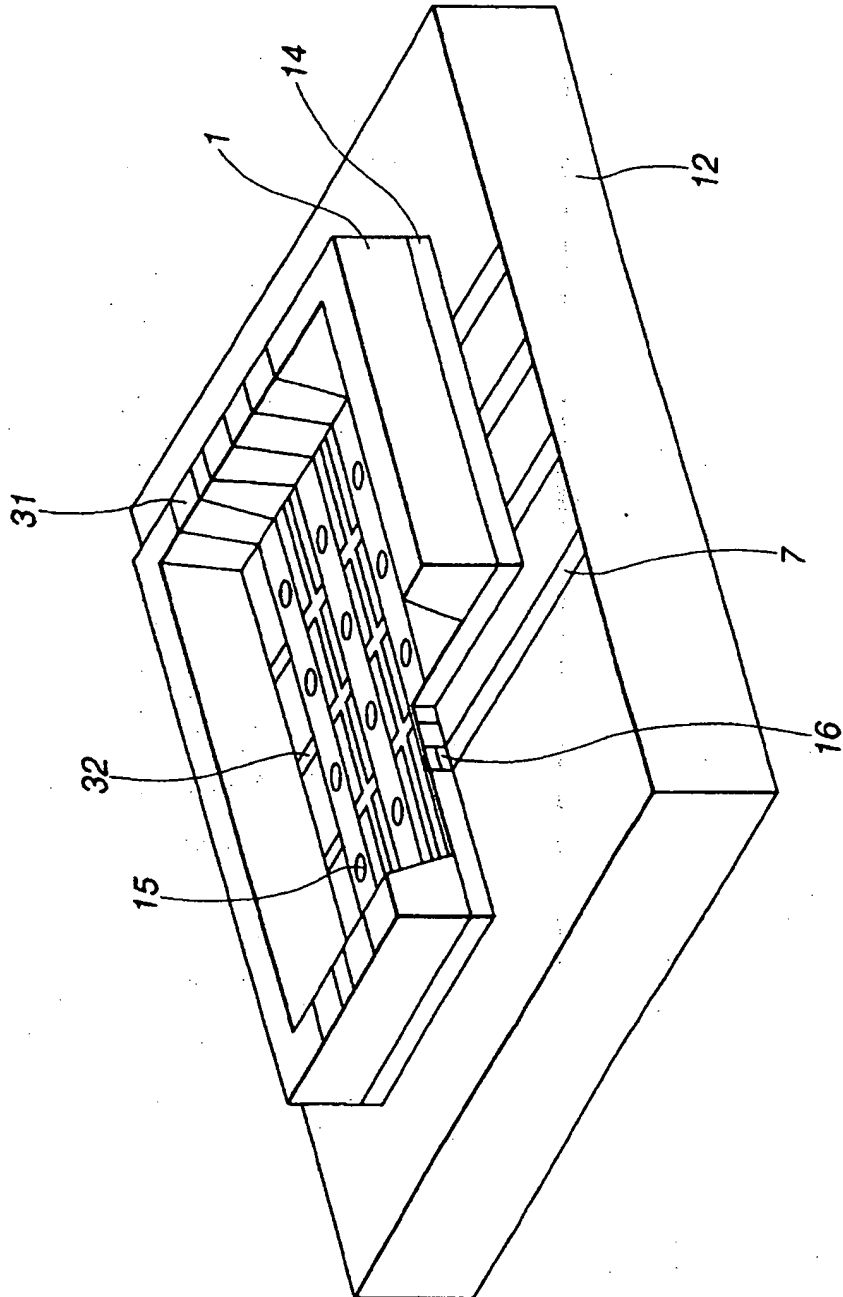


FIG.6

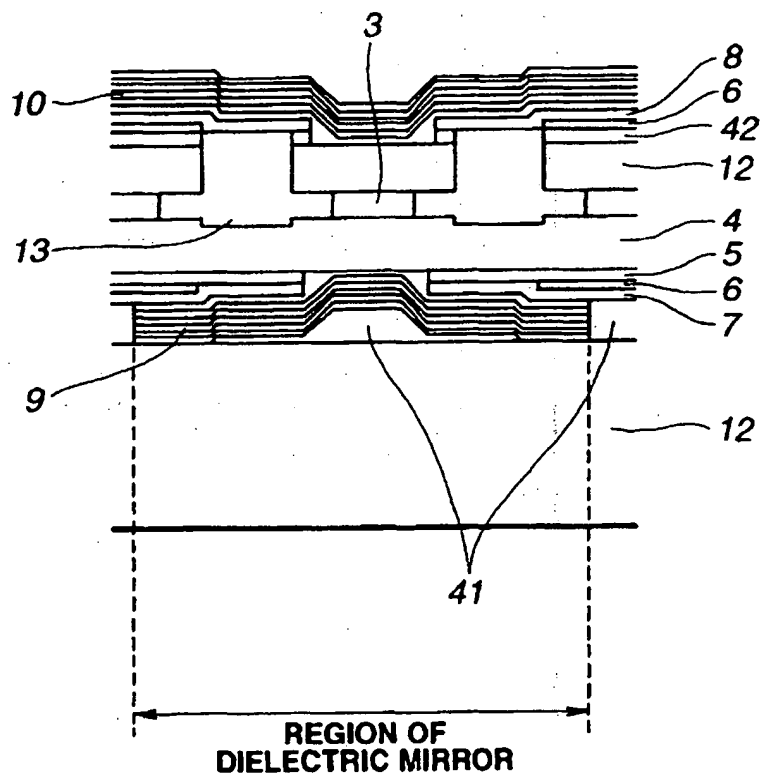


FIG.7

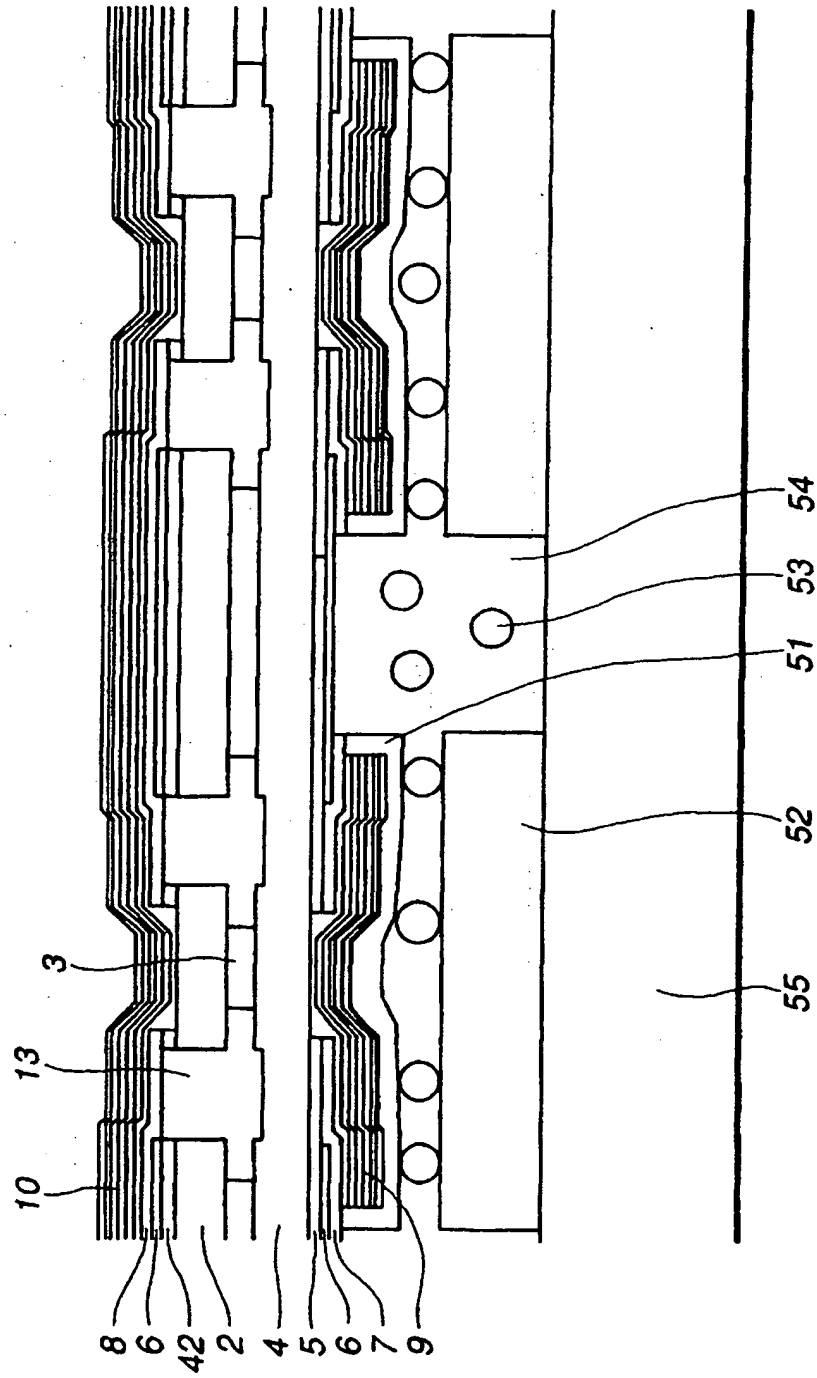


FIG.8

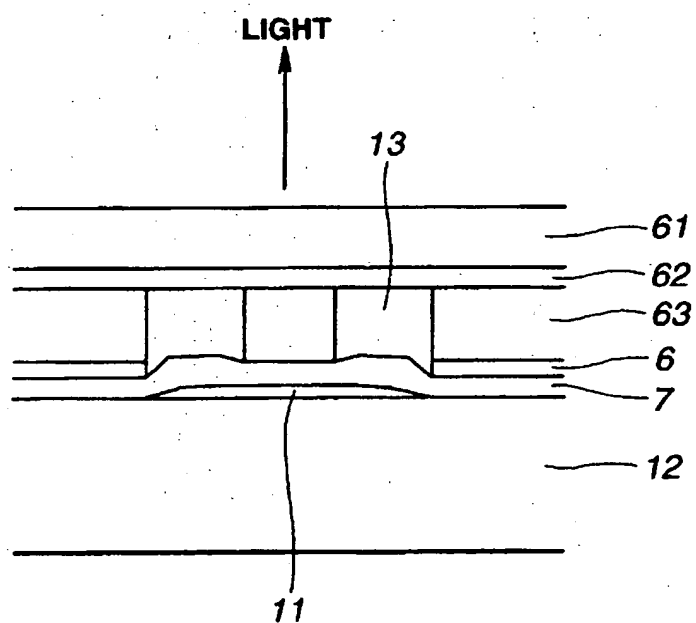


FIG.9

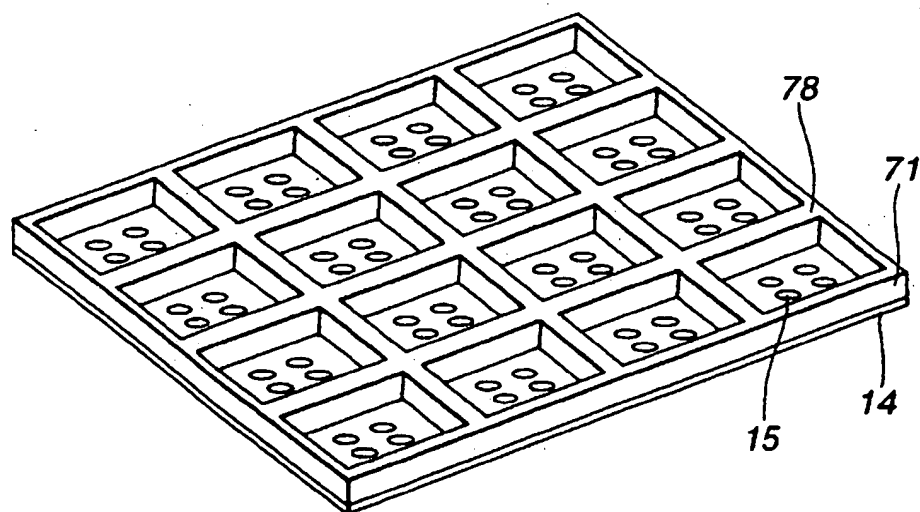


FIG.10

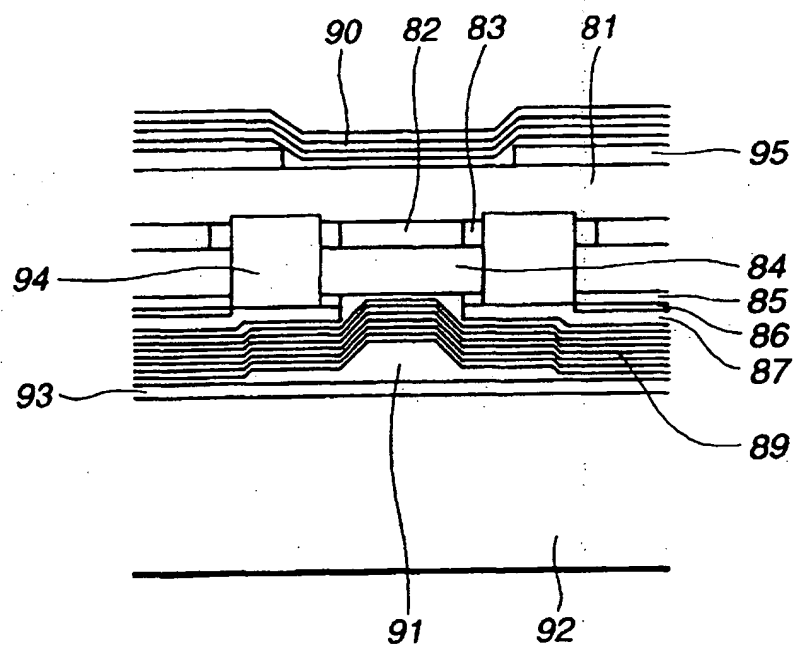
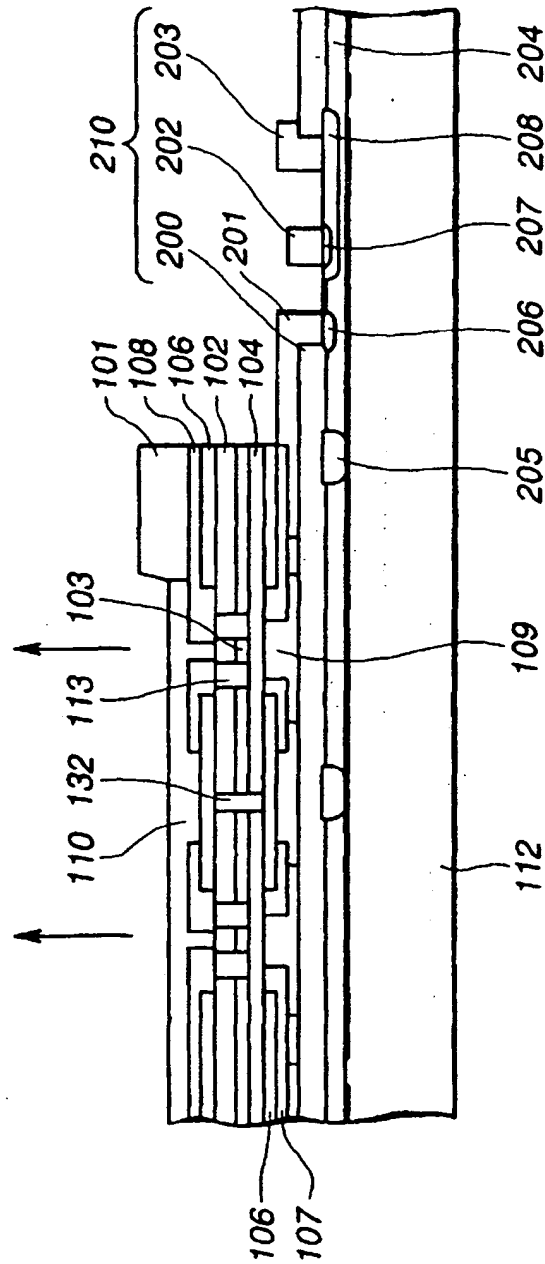


FIG.11





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 11 7860

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP 0 499 659 A (SIEMENS AG) 26 August 1992 * column 4, line 12-19 *	1,2,5-7, 10, 12-14, 18,23, 24,26-30	H01S3/25 H01L33/00 G09G3/14
A	US 5 453 405 A (MCCLELLAND ROBERT W ET AL) 26 September 1995 * the whole document *	1,23	
A	EP 0 704 947 A (MATSUSHITA ELECTRIC IND CO LTD) 3 April 1996 * the whole document *	1,23	
D,A	PATENT ABSTRACTS OF JAPAN vol. 097, no. 012, 25 December 1997 & JP 09 223848 A (NIPPON TELEGR & TELEPH CORP <NTT>), 26 August 1997 * abstract *	1,23	
A	UCHIYAMA S ET AL: "TWO-DIMENSIONAL ARRAY OF GAINASP/INP SURFACE-EMITTING LASERS" ELECTRONICS LETTERS, vol. 21, no. 4, 14 February 1985, pages 162-164, XP000709768 * figure 1 *	1,23	
The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H01S H01L G09G
Place of search		Date of completion of the search	Examiner
THE HAGUE		7 January 1999	Claessen, L
CATEGORY OF CITED DOCUMENTS			
<p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p>			

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 98 11 7860

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

07-01-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0499659 A	26-08-1992	JP 5090716 A	09-04-1993
US 5453405 A	26-09-1995	US 5300788 A	05-04-1994
		WO 9213363 A	06-08-1992
		US 5377031 A	27-12-1994
		US 5539550 A	23-07-1996
		US 5583335 A	10-12-1996
		US 5499124 A	12-03-1996
		US 5757445 A	26-05-1998
		US 5258325 A	02-11-1993
		US 5376561 A	27-12-1994
		US 5256562 A	26-10-1993
		US 5331149 A	19-07-1994
EP 0704947 A	03-04-1996	JP 2795627 B	10-09-1998
		JP 8153935 A	11-06-1996
		US 5796714 A	18-08-1998

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☒ FADED TEXT OR DRAWING
- ☒ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☐ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☒ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.